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(71) Applicant: **SONY CORPORATION**
Tokyo (JP)

(72) Inventor: Keiji, Mabuchi
Shinagawa-ku, Tokyo (JP)

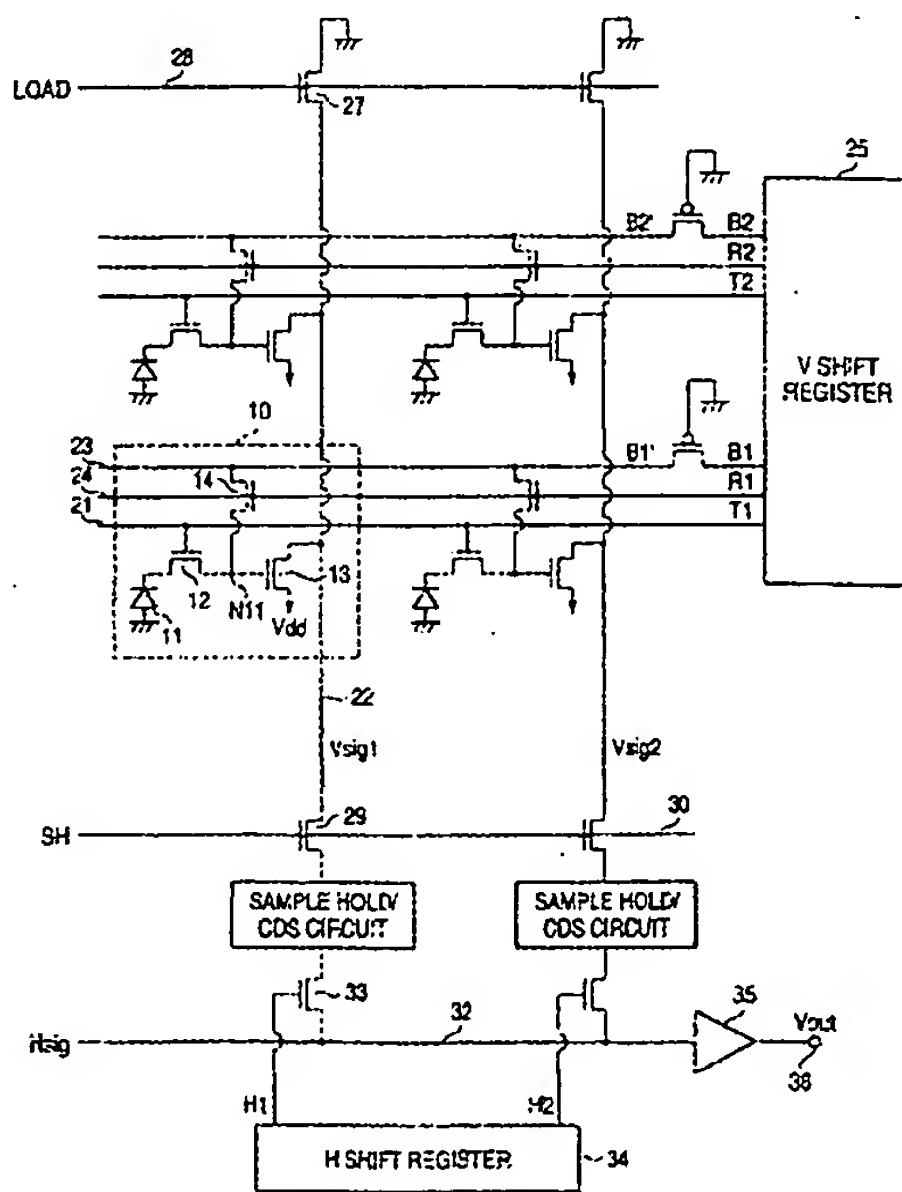
(74) Representative: Thévenet, Jean-Bruno et al
Cabinet Beau de Loménie 158, rue de l'Université
75340 Paris Cédex 07 (FR)

(54) Solid-state image pickup device and camera system

(57) In a MOS type solid-state image pickup device in which unit pixels (10) each including a photodiode (11), a transfer transistor (12) for transferring the signal of the photodiode to a floating node (N11), an amplifying transistor (13) for outputting the signal of the floating node to a vertical signal line (22), and a reset transistor (14) for resetting the floating node are arranged in a ma-

trix form, a P-type MOS transistor (26) is connected between a drain line (23) to which the drain of the reset transistor is connected and a V shift register (25) for selectively supplying the reset voltage to the drain line, and the potential of the floating node is set to the channel voltage of the P-type MOS transistor at the non-selection time.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a solid-state image pickup device and a camera system using the same, and particularly to an X-Y address type solid-state image pickup device which is represented by a MOS type solid-state image pickup device, and a camera system using the solid-state image pickup device as an image pickup device.

2. Description of the Related Art

[0002] As an X-Y address type solid-state image pickup device such as a MOS type solid-state image pickup device has been known an image pickup device including many unit pixels arranged in a matrix form, each unit pixel being constructed by three transistors. Fig. 4 shows the construction of each unit pixel of the above image pickup device. As is apparent from Fig. 4, each unit pixel 100 comprises a photodiode (PD) 101, a transfer transistor 102, an amplifying transistor 103 and a reset transistor 104.

[0003] According to a MOS type solid-state image pickup device using the above pixel array, the potential of a floating node N101 is set to low level (hereinafter referred to as "L level") on the basis of a signal input from a drain line 105 through the reset transistor 104 during a non-selection period for which a line is non-selected, and the potential of the floating node N101 is set to high level (hereinafter referred to as "H level") when the line is selected.

[0004] As described above, in the conventional MOS type solid-state image pickup device including unit pixels each of which comprises three transistors, the potential of the floating node N101 is set to the L level (0V) during the non-selection period, so that electrons may leak from the floating node N101 into the photodiode 101, resulting in occurrence of noises.

SUMMARY OF THE INVENTION

[0005] The present invention has been implemented in view of the foregoing problem of the conventional solid-state image pickup device, and has an object to provide a solid-state image pickup device which can prevent electrons from leaking from a floating node to a photodiode to thereby reduce noises caused by the leakage of the electrons. The present invention has another object to provide a camera system using the solid-state image pickup device thus constructed as an image pickup device.

[0006] In order to attain the above object, according to a first aspect of the present invention, a solid-state image pickup device having unit pixels arranged in a

matrix form, each unit pixel comprising a photoelectrical conversion element, a transfer transistor for transferring a signal of the photoelectrical conversion element to a floating node, an amplifying transistor for outputting a signal of the floating node to a signal line, and a reset transistor for resetting said floating node, is characterized in that a P-type MOS transistor is connected between a wire to which a main electrode of the reset transistor at the opposite side to the floating node is connected and a driving circuit for selectively applying a reset voltage to the wire.

[0007] According to a second aspect of the present invention, there is provided a camera system using the above solid-state image pickup device as an image pickup device.

[0008] According to the solid-state image pickup device of the first aspect of the present invention and the camera system of the second aspect of the present invention, when the reset voltage is output from the driving circuit, the P-type MOS transistor is conducted to thereby apply the reset voltage to the wire. The reset voltage is supplied through the reset transistor to the floating node to thereby reset the potential of the node concerned. On the other hand, when no reset voltage is output from the driving circuit, the channel voltage of the P-type MOS transistor is applied to the wire. When the reset transistor is conducted, the potential of the floating node is determined by the channel voltage of the P-type MOS transistor, and thus it is not equal to 0V. Therefore, the leakage of charges from the floating node through the transfer transistor to the photoelectrical conversion element can be prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

Fig. 1 is a circuit diagram showing the construction of a MOS-type solid-state image pickup device according to an embodiment of the present invention; Fig. 2 is a timing chart showing the operation of the MOS-type solid-state image pickup device according to this embodiment;

Fig. 3 is a block diagram showing an example of the construction of a camera system according to the present invention; and

Fig. 4 is a diagram showing the construction of a unit pixel to describe the problem of the conventional technique.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] Preferred embodiments according to the present invention will be described hereunder with reference to the accompanying drawings.

[0011] Fig. 1 is a circuit diagram showing the construction example of a MOS-type solid-state image pickup

up device according to a first embodiment of the present invention.

[0012] In the MOS-type solid-state image pickup device, many unit pixels are arranged in a matrix form, however, in order to simplify the illustration, these unit pixels are simply illustrated as a pixel array of 2 lines x 2 columns.

[0013] In Fig. 1, a unit pixel 10 is designed in a three-transistor structure including three N-type MOS transistors, that is, a transfer transistor 12, an amplifying transistor 13 and a reset transistor 14 in addition to a photoelectrical conversion element such as a photodiode 11.

[0014] In the pixel array as described above, the photodiode 11 photoelectrically converts incident light to signal charges (for example, electrons) having the charge amount corresponding to the light amount of the incident light and accumulates the signal charges.

[0015] The transfer transistor 12 is connected between the cathode of the photodiode 11 and a floating node N11, and the gate thereof is connected to a vertical selection line 21. The transfer transistor 12 has a function of transferring the signal charges accumulated in the photodiode 11 to the floating node N11 when it is set to a conduction state (ON).

[0016] The amplifying transistor 13 is connected between a vertical signal line 22 and a power source Vdd, and the gate thereof is connected to the floating node N11. It has a function of outputting the potential of the floating node N11 to the vertical signal line 22.

[0017] With respect to the reset transistor 14, the drain thereof (one main electrode) is connected to a drain line (wire) 23, the source thereof (the other main electrode) is connected to the floating node N11, and the gate thereof is connected to the reset line 24, and with this connection arrangement, it has a function of resetting the potential of the floating node N11.

[0018] In a pixel area (image pickup area) in which these unit pixels 10 are arranged in a matrix form, respective three lines of the vertical selection line 21, the drain line 23 and the reset line 24 are wired in the horizontal (H) direction (the right-and-left direction in Fig. 1) every line of the pixel array, and the respective vertical signal lines 22 are wired in the vertical (V) direction (the up-and-down direction) every column.

[0019] The vertical selection line 21 and the reset line 24 are directly connected to the respective output terminals of a V shift register 25 constituting the vertical driving circuit, which outputs a vertical selection pulse T and a reset pulse R every line. The drain line 23 is connected to each reset voltage output terminal of the V shift register 25 through each P-type MOS transistor 26 every line. The gate of the P-type MOS transistor 26 is grounded.

[0020] At the upper side of the pixel area, a load transistor 27 comprising an N-type MOS transistor is connected between one end of the vertical signal line 22 and the ground every column. The gate of the load transistor 27 is connected to a load (Load) line 28 and it serves as a constant current source.

sistor 27 is connected to a load (Load) line 28 and it serves as a constant current source.

[0021] At the lower side of the pixel area, one terminal (one main electrode) of a sample hold (SH) switch 29 comprising an N-type MOS transistor is connected to the other end of the vertical signal line 22. The control terminal (gate) of the sample hold switch 29 is connected to an SH line 30.

[0022] The input terminal of a sample hold/CDS (Correlated Double Sampling) circuit 31 is connected to the other terminal (the other main electrode) of the sample hold switch 29. The sample hold/CDS circuit 31 samples and holds the potential Vsig of the vertical signal line 22 and conducts the correlated double sampling (CDS). Here, the correlated double sampling means the processing of sampling two voltage signals input time-serially and then outputting the differential value therebetween.

[0023] A horizontal selection switch 33 comprising an N-type MOS transistor is connected between the output terminal of the sample hold/CDS circuit 31 and the horizontal signal line 32. Horizontal scanning pulses H (H1, H2, ...) that are successively output during the horizontal scanning operation are supplied from an H shift register 34 constituting a horizontal driving circuit to the control terminal (gate) of the horizontal selection switch 33.

[0024] When the horizontal scanning pulses H are supplied and thus the horizontal selection switch 33 is turned on, the signal which has been subjected to CDS in the sample hold/CDS circuit 31 is read out through the horizontal selection switch 33 to the horizontal signal line 32. The signal Hsig thus read out is led out as an output signal Vout from the output terminal 36 through an output amplifier 35 connected to one end of the horizontal signal line 32.

[0025] Next, the operation of the MOS type solid-state image pickup device according to this embodiment will be described with reference to the timing chart of Fig. 2. In this case, the description will be made while paying attention to the pixel at the lower left side of Fig. 1.

[0026] First, at the non-selection time (when the unit pixel is not selected), the potential of the floating node N11 is set to 0.5V. At this time, the power source voltage Vdd, for example, 3.0V is output as a reset voltage B1 from the V shift register 25 and thus the P-type MOS transistor 26 is conducted, so that the potential B1' of the drain line 23 is also set to the power source voltage Vdd.

[0027] When a load (Load) signal to be applied to the load line 28 is set to 1.0V, for example, and then a reset signal R1 having H level is output from the V shift register 25, the floating node N11 is connected to the drain line 23 through the reset transistor 14 because the reset transistor 14 is conducted. Therefore, the potential of the floating node N11 is reset to the H level determined by the channel voltage of the reset transistor 14 (for example, 2.5V), whereby the gate potential of the amplifying transistor 27 is connected to a load (Load) line 28 and it serves as a constant current source.

ing transistor 13 is also set to 2.5V.

[0028] The potential V_{sig1} of the vertical signal line 22 is determined by the highest one of the gate voltages of the amplifying transistors of many pixels which are arranged in the vertical direction and connected to the vertical signal line 22, so that the potential V_{sig1} of the vertical signal line 22 is determined by the potential of the floating node N11. Specifically, the amplifying transistor 13 forms a source follower in combination with a load transistor 27, and the output voltage thereof appears as the pixel potential V_{sig1} on the vertical signal line 22. The potential V_{sig1} at this time is set as a voltage having reset level. The reset-level voltage is input through the sample hold switch 29 to the sample hold/CDS circuit 31.

[0029] Subsequently, a vertical selection pulse T1 output from the V shift register 25 is set to H level. In this case, the transfer transistor 12 is conducted, photoelectrical conversion is conducted in the photodiode 11, and signal charges (in this case, electrons) accumulated are transferred (read) to the floating node N11, whereby the gate potential of the amplifying transistor 13 is varied in the negative direction in accordance with the signal amount of the signal charges read out from the photodiode 11 to the floating node N11, and this variation induces variation of the potential V_{sig1} of the vertical signal line 22.

[0030] The potential V_{sig1} at this time corresponds to the voltage having the original signal level. This signal level voltage is input through the sample hold switch 29 to the sample hold/CDS circuit 31. The sample hold/CDS circuit 31 carries out the processing of differentiating the previous reset level voltage and the current signal level voltage and holding the differential voltage thus achieved.

[0031] Subsequently, the reset voltage B1 output from the V shift register 25 is set to 0V. At this time, the reset voltage B1' supplied through the drain line 23 to the pixel 10 is not equal to 0V, but it is determined by the channel voltage of the P-type MOS transistor 26, for example, it is equal to 0.5V.

[0032] If the reset signal R1 having the H level is output from the V shift register 25 under the above state, the reset transistor 14 is conducted, so that the floating node N11 is linked to the drain line 23 through the reset transistor 14, and the potential thereof is equal to the potential of the drain line 23, that is, 0.5V. Therefore, the pixel 10 is restored to the non-selection state.

[0033] Under the non-selection state, the potential of the floating node N11 is not equal to 0V, but 0.5V, and thus electrons are prevented from leaking through the transfer transistor 12 to the photodiode 11. Here, the potential of the floating node N11 is set to 0.5V by the action of the P-type MOS transistor 26 disposed between the reset voltage output terminal of the V shift register 25 and the drain line 23.

[0034] All the pixels on the first line are simultaneously driven through the above sequential operation, and the

signals of one line are simultaneously held (stored) in the sample hold/CDS circuits 31. Thereafter, the processing enters a next photoelectric conversion (exposure) and photoelectrons accumulation period in the photodiode 11. As described in the timing chart of Fig. 2, the H shift register 34 starts the horizontal scanning operation during the photoelectron accumulation period, and successively outputs the horizontal scanning pulses H1, H2, ..., whereby the horizontal selection switches 33 are successively conducted to successively lead the signals held in the sample hold/CDS circuits 31 to the horizontal signal line 32.

[0035] When the same operation is carried out on the pixels on the second line, the pixel signals of the pixels on the second line are read out. Subsequently, the pixel signals of all the lines can be read out by the successive vertical scanning operation of the V shift register 25, and the signals of all the pixels can be read out by the successive horizontal scanning operation of the H shift register 34 every line.

[0036] As described above, in the MOS type solid-state image pickup device having the three-transistor structure in which each unit pixel 10 has the transfer transistor 12, the amplifying transistor 13 and the reset transistor 14, the P-type MOS transistor 26 is connected between the reset voltage output terminal of the V shift register 25 and the drain line 23, whereby the potential of the floating node N11 is equal to 0.5V, for example. Therefore, electrons can be prevented from being leaked through the transfer transistor 12 to the photodiode 11.

[0037] Accordingly, the noises caused by the leakage of electrons from the floating node N11 to the photodiode 11 can be suppressed. Further, the present invention can be implemented by a simple circuit construction in which only one MOS transistor is added every line, and thus the circuit scale may be extremely small. In addition, the present invention does not need any current flow that has been hitherto required in the case of a resistance-dividing manner when an intermittent voltage (in this embodiment, 0.5V) is generated. Therefore, increase of power consumption can be suppressed.

[0038] In the above embodiment, the P-type MOS transistor 26 is connected between the reset voltage output terminal of the V shift register 25 and the drain line 23, and the gate thereof is grounded. However, the present invention is not limited to this construction. The P-type MOS transistor is not required to have a gate, but it may be equipped with a P-type potential-constant channel. There has been achieved an inventor's experiment result showing that the channel voltage is preferably set to 0.4V to 0.7V in order to prevent the leakage of electrons to the photodiode and suppress the reduction of the voltage margin.

[0039] Fig. 3 is a block diagram schematically showing the construction of a camera system according to another embodiment of the present invention.

[0040] The camera system includes an image pickup

device 41, an optical system for guiding incident light to the pixel area of the image pickup device 41, for example, a lens 42 for focusing the incident light (Image light) onto the imaging face, a driving circuit 43 for driving the image pickup device 41, a signal processing circuit 44 for processing the output signal of the image pickup device 41.

[0041] This camera system uses as the image pickup device 41 the solid-state image pickup device according to the first embodiment, that is, the MOS-type solid-state image pickup device having the three-transistor structure in which each unit pixel 10 includes not only the photodiode 11, but also the transfer transistor 12, the amplifying transistor 13 and the reset transistor 14, and the P-type MOS transistor 26 is connected between the reset voltage output terminal of the V shift register 25 and the drain line 23.

[0042] The driving circuit 43 has a timing generator (not shown) for generating various timing signals containing a start pulse and a clock pulse to drive the V shift register 25 and the H shift register 34 shown in Fig. 1, and drives the image pickup device (MOS type solid-state image pickup device) 41 in order to implement the driving operation described in the above-described example of the operation. The signal processing circuit 44 carries out various signal processing on the output signals Vout of the MOS-type solid-state image pickup device 41 and outputs the processed signals as video signals.

[0043] As described above, according to the camera system of this embodiment, the MOS-type solid-state image pickup device as described above is used as the image pickup device 41, so that the MOS-type solid-state image pickup device concerned can reduce the noises due to the leakage of electrons from the floating nodes to the photodiodes without increasing the power consumption with a small circuit scale. Therefore, a high image quality pickup image can be achieved with small circuit scale/low power consumption and with little noise.

[0044] As described above, according to the present invention, in a solid-state image pickup device in which a unit pixel has a photoelectrical conversion element, a transfer transistor for transferring a signal of the photoelectrical conversion element to a floating node, an amplifying transistor for outputting a signal of the floating node to a signal line, and a reset transistor for resetting said floating node, a P-type MOS transistor is connected between a wire to which a main electrode of the reset transistor at the opposite side to the floating node is connected and a driving circuit for selectively applying a reset voltage to the wire. Therefore, the leakage of the charges from the floating node to the photoelectrical conversion element can be prevented, and thus the noises due to the leakage can be reduced.

Claims

1. A solid-state image pickup device having:
unit pixels arranged in a matrix form, each pixel unit comprising a photoelectrical conversion element, a transfer transistor for transferring a signal of said photoelectrical conversion element to a floating node, an amplifying transistor for outputting a signal of said floating node to a signal line, a reset transistor for resetting said floating node, and a P-type MOS transistor, wherein said P-type MOS transistor is connected between a wire to which a main electrode of said reset transistor at the opposite side to said floating node is connected and a driving circuit for selectively applying a reset voltage to said wire.
2. The solid-state image pickup device as claimed in claim 1, wherein the channel voltage of said P-type MOS transistor is equal to 0.4V to 0.7V.
3. A camera system comprising:
a solid-state image pickup device in which a unit pixel has a photoelectrical conversion element, a transfer transistor for transferring a signal of said photoelectrical conversion element to a floating node, an amplifying transistor for outputting a signal of said floating node to a signal line, a reset transistor for resetting said floating node, a P-type MOS transistor, an optical system for guiding incident light to said image pickup portion of said solid-state image pickup device; and a signal processing circuit for processing the output signal of said solid-state image pickup device, wherein said P-type MOS transistor, is connected between a wire to which a main electrode of said reset transistor at the opposite side to said floating node is connected and a driving circuit for selectively applying a reset voltage to said wire.

FIG. 1

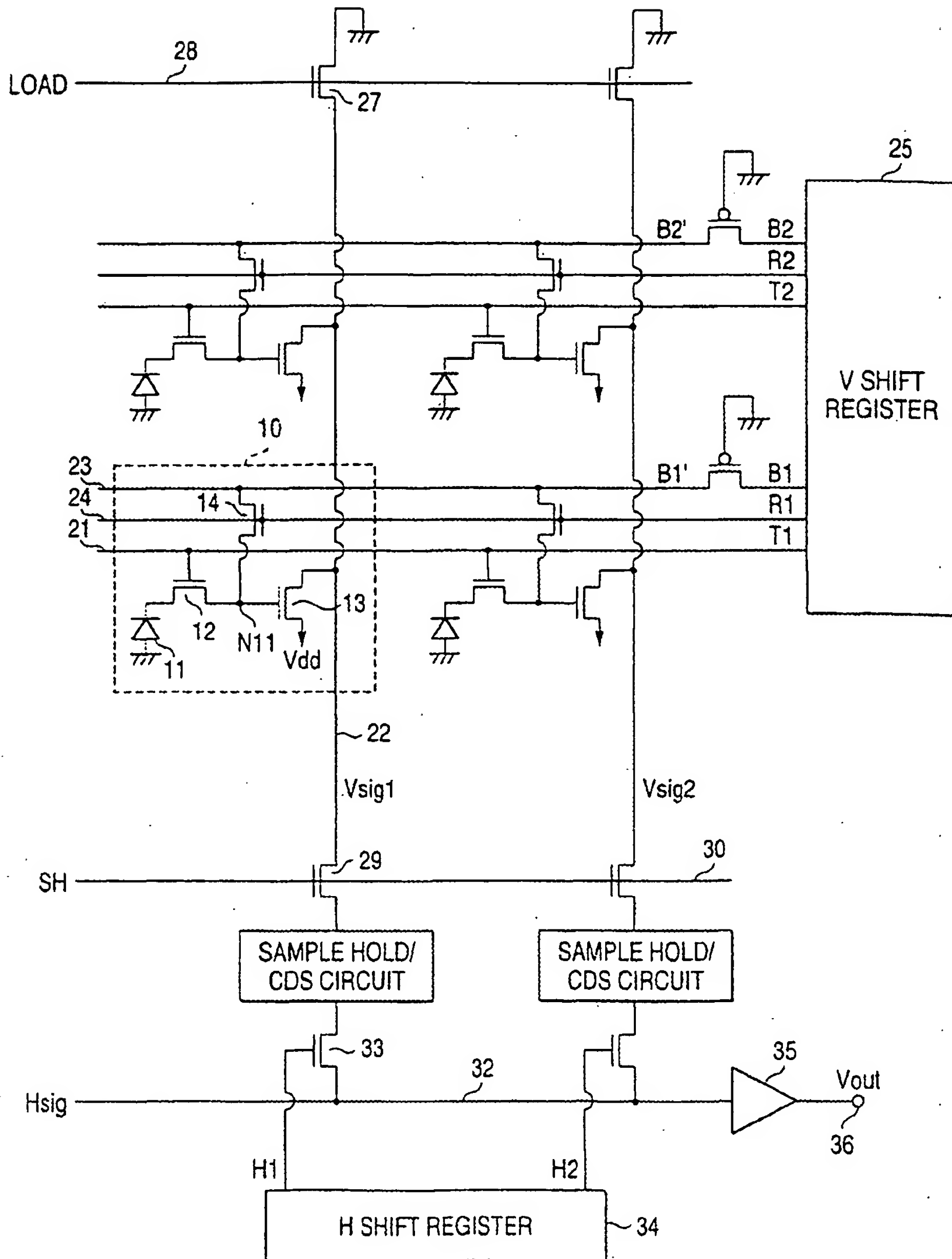


FIG. 2

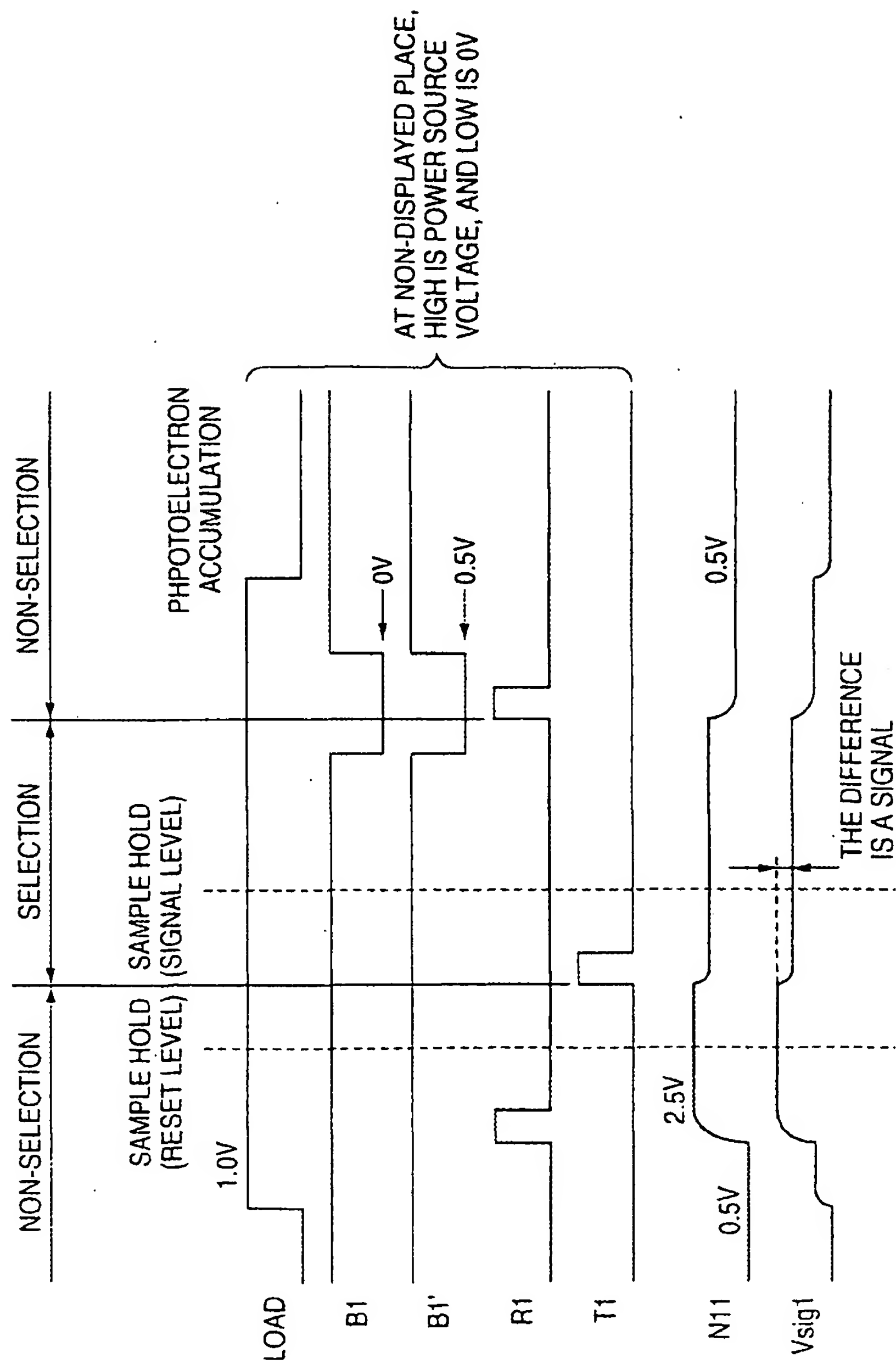


FIG. 3

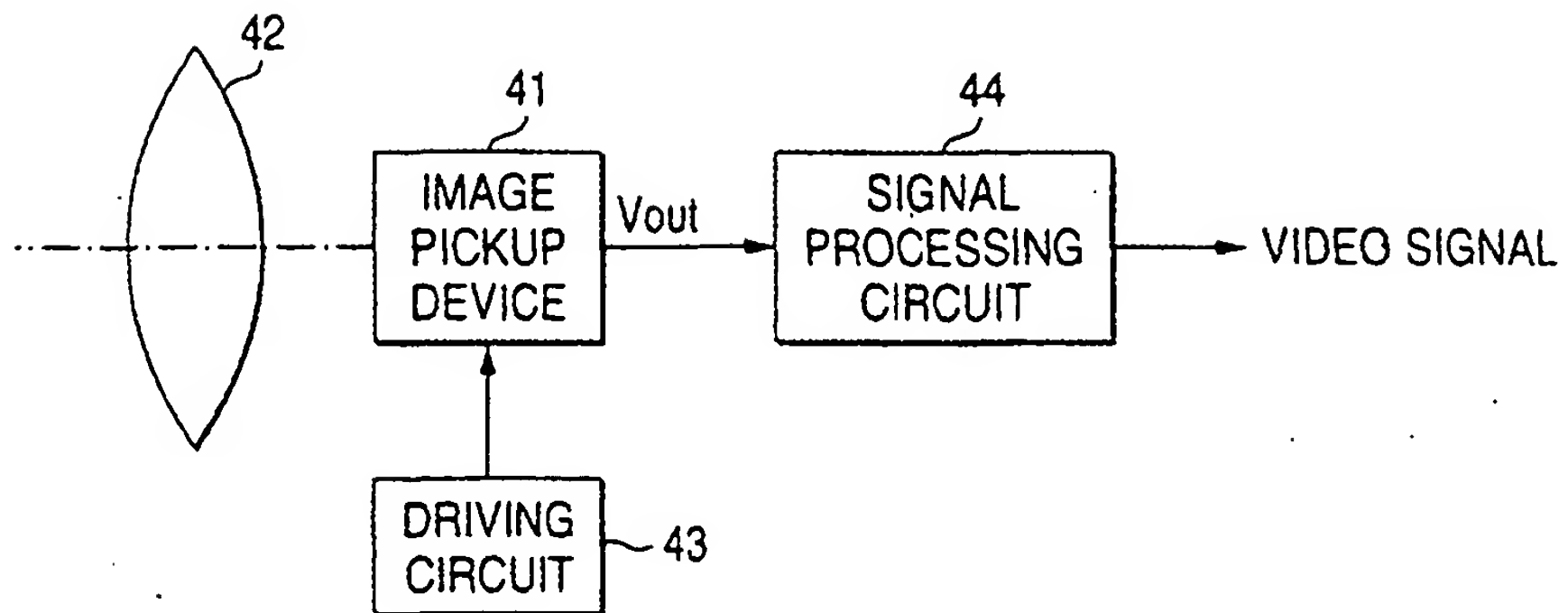
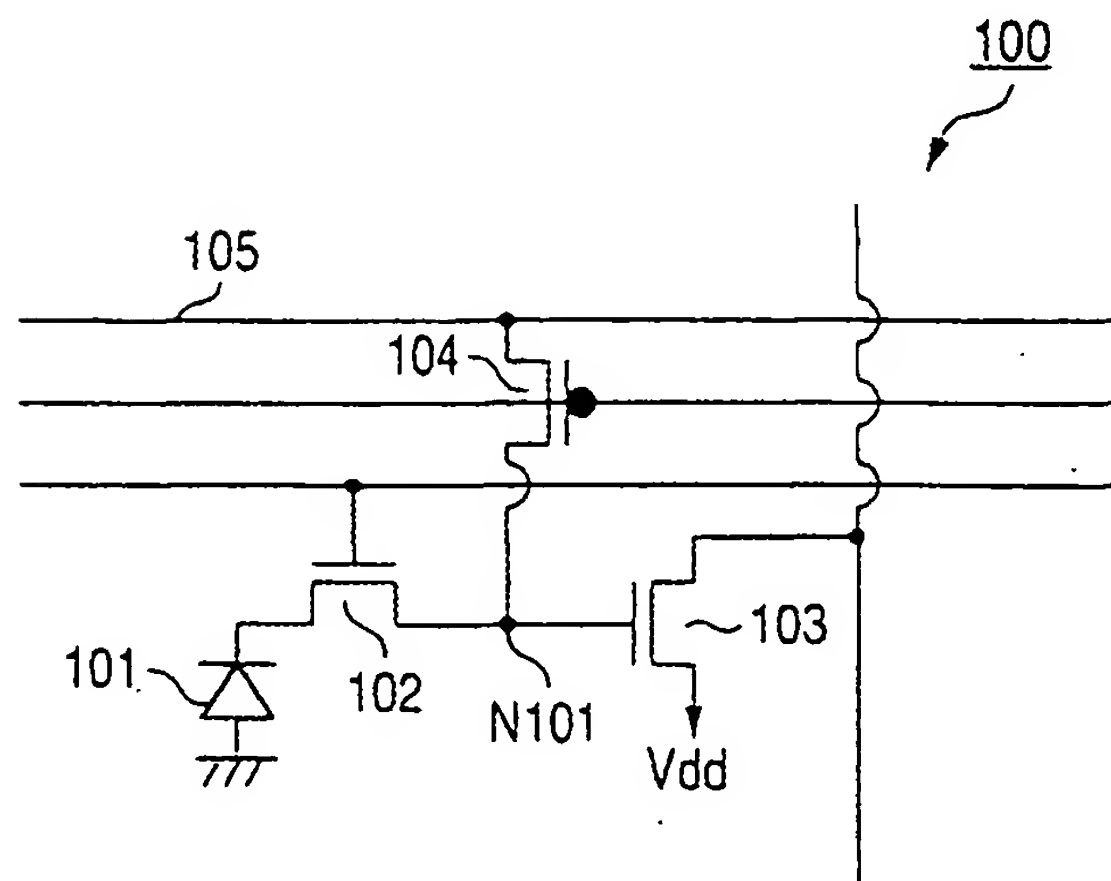


FIG. 4





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EUROPEAN SEARCH REPORT

Application Number
EP 01 40 2091

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 4 December 2001	Examiner Bequet, T
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**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 01 40 2091

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